16. The semiconductor device as claimed in claim 1, wherein the active areas have a width of about 8 μm, and the second sections have a width of about 8 μm.

17. The semiconductor device as claimed in claim 1, wherein the first trenches have a depth of about 1200 Å.

18. The semiconductor device as claimed in claim 1, wherein the substantially transparent layer comprises silicon dioxide.

19. A semiconductor device, comprising:

a set of alignment marks on a main surface of a semiconductor substrate, each alignment mark having an upper surface substantially flush with the main surface;

a dummy topography area, on the main surface peripheral to the set of alignment marks, comprising a plurality of second trenches spaced apart by second uprights having an upper surface substantially flush with the main surface, the dummy topography area extending a predetermined distance away from the set of alignment marks; and

a substantially transparent layer having a substantially planar upper surface formed on the set of alignment marks and on the dummy topography area.

20. The semiconductor device as claimed in claim 19, wherein the second trenches and second uprights have approximately the same width.

21. The semiconductor device as claimed in claim 20, wherein the width of the second trenches and second uprights is about equal to the minimum width according to the design rule for the semiconductor device.

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